Am335x Pru Icss Reference Guide Rev A

AM335x PRU-ICSS Debug

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3.5. PRU-ICSS / PRU_ICSSG — Processor SDK Linux Documentation
Simple PID Control Reference Design With PRU®-ICSS Through Web Interface Thermal Printing with the PRU-ICSS on the BeagleBone Black Reference Design Simple Open Real-Time Ethernet (SORTE) Device With PRU-ICSS Reference Design EnDat 2.2 System Reference Design. Evaluation Hardware . can be ordered from ti.com. PRU Cape; Getting Started Guide

PRU-ICSS - Texas Instruments Wiki
AM335x PRU-ICSS Reference Guide The documentation on the subsystem is here. TI does not support this subsystem and all questions/inquires/problems should be directed to the community. Example for the first PRU version (Ti AM18XX and other DSP) http://www.ti.com/tool/sprc940

Ti AM33XX PRUSSv2 - eLinux.org
----- The AM335x PRU Package includes: Documentation: AM335x PRU-ICSS overview slides AM18x to AM335x PRU software migration guide AM335x PRU Linux Application Driver documentation CCS AM335x PRU Debugger training slides AM335x_PRU_ICSS gel file for use with CCS AM335x PRU Debugger PRU software (pru_sw): Utils: PASM (PRU assembler) binary PASM ...

GitHub - beagleboard/am335x_pru_package
As you have already discovered, the PRU GPI/Os are uni-directional (not bi-directional) and while some of the PRU GPIs and GPOs are muxed on the same pin, the PRU does not have privileges to write to the AM335x Control Registers to change the pinmuxing. However, you could use the PRU Digital I/Os to achieve a high impedance output.

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As seen from the screenshot the interrupt number for PRU_ICSS_EVTOUT_0 on AM335x is 20, so the interrupt number that must be configured for this in application should be 20 if the platform is AM335x. This is done in the following line (defined in main.c)

ICSS EMAC LLD developers guide - Texas Instruments Wiki
Parameters Arm MHz (Max.) 800 Serial I/O CAN, I2C, SPI, UART, USB Co-processor(s) PRU-ICSS Graphics acceleration 1 3D Ethernet MAC 2-Port 10/100 PRU EMAC, 2-Port 1Gb Switch Security enabler Cryptographic acceleration, Debug security, Initial secure programming, Secure boot, Software IP protection Operating temperature range (C)-40 to 105 Display type 1 LCD DRAM DDR2, DDR3, DDR3L, LPDDR Arm CPU ...

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The description of the HIEISR register (AM335x PRU-ICSS Reference Guide chapter 6.4.9) is a bit unclear for me: The Host Interrupt Enable Indexed Set Register allows enabling a host interrupt output. The host interrupt. to enable is the index value written.

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Refer to the AM335x PRU ICSS Reference Guide about these register values. Each register is directly addressable as a memory segment, given by the Local Data Memory Map in the Reference Manual. This shows the IEP timer starts at address 0x0002_E000. The memory offset of the GLOBAL_CFG register is 0h (so no offset).

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Programmable Real-Time Unit and Industrial ... - TI.com
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