Hardware Verification With C : A Practitioner's Handbook: A Practitioner's Approach

This volume contains the proceedings of the 10th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS 2004). TACAS 2004 took place in Barcelona, Spain, from March 29th to April 2nd, as part of the 7th European Joint Conferences on Theory and Practice of Software (ETAPS 2004), whose aims, organization, and history are detailed in a foreword by the ETAPS Steering Committee Chair, Jos ? e Luiz Fiadeiro. TACAS is a forum for researchers, developers, and users interested in ri- rously based tools for the construction and analysis of systems. The conference serves to bridge the gaps between di?erent communities including, but not - mited to, those devoted to formal methods, software and hardware veri?cation, static analysis, programming languages, software engineering, real-time systems, and communication protocols that share common interests in, and techniques for, tool development. In particular, by providing a venue for the discussion of common problems, heuristics, algorithms, data structures, and methodologies, TACAS aims to support researchers in their quest to improve the utility, rel- bility, ?exibility, and e?ciency of tools for building systems.
TACASseekstheoreticalpaperswithaclearlinktotoolconstruction,papers describingrelevantalgorithmsandpracticalaspectsoftheirimplementation,-pers giving descriptions of tools and associated methodologies, and case studies with a conceptual message.

This book provides comprehensive coverage of verification and debugging techniques for embedded software, which is frequently used in safety critical applications (e.g., automotive), where failures are unacceptable. Since the verification of complex systems needs to encompass the verification of both hardware and embedded software modules, this book focuses on verification and debugging approaches for embedded software with hardware dependencies. Coverage includes the entire flow of design, verification and debugging of embedded software and all key approaches to debugging, dynamic, static, and hybrid verification. This book discusses the current, industrial embedded software verification flow, as well as emerging trends with focus on formal and hybrid verification and debugging approaches.

This book presents 8 papers accompanying the lectures of leading researchers given at the 6th edition of the International School on Formal Methods for the Design of Computer, Communication and Software Systems (SFM 2006). SFM 2006 was devoted to formal techniques for hardware verification and covers several aspects of the hardware design process, including hardware design languages and simulation, property specification formalisms, automatic test pattern generation, symbolic trajectory evaluation, and more.

This volume contains the proceedings of CHARME 2001, the Eleventh Advanced Research Working Conference on Correct Hardware Design and Veri?cation Methods. CHARME 2001 is the 11th in a series of working conferences devoted to the development and use of leading-edge formal techniques and tools for the design and veri?cation of hardware and hardware-like systems. Previous events in the 'CHARME' series were held in Bad Herrenalb (1999), Montreal (1997), Frankfurt (1995), Arles (1993), and Torino (1991). This series of meetings has been organized in cooperation with IFIP WG 10.5 and WG 10.2. Prior meetings, stretching backto the earliest days of formal hardware veri?cation, were held under various names in Miami (1990), Leuven (1989), Glasgow (1988), Grenoble (1986), Edinburgh (1985), and Darmstadt (1984). The convention is now well-established whereby the European CHARME conference alternates with its biennial counterpart, the International Conference on Formal Methods in Computer-Aided Design (FMCAD), which is held on even-numbered years in the USA. The conference tookplace during 4–7 September 2001 at the Institute for System Level Integration in Livingston, Scotland. It was co-hosted by the - stitute and the Department of Computing Science of Glasgow University and co-sponsored by the IFIP TC10/WG10.5 Working Group on Design and En- neering of Electronic Systems. CHARME 2001 also included a scienti?c session and social program held jointly with the 14th International Conference on Th- rem Proving in Higher Order Logics (TPHOLs), which was co-located in nearby Edinburgh.

Formal Hardware Verification
A Systems Approach to Cyber Security
13th International Haifa Verification Conference, HVC 2017, Haifa, Israel, November 13-15, 2017, Proceedings
Comprehensive Functional Verification
Scalable Hardware Verification with Symbolic Simulation
Verification by Error Modeling

Verification is increasingly complex, and SystemVerilog is one of the languages that the verification community is turning to. However, no language by itself can guarantee success without proper techniques. Object-oriented programming (OOP), with its focus on managing complexity, is ideally suited to this task. With this handbook—the first to focus on applying OOP to SystemVerilog—we'll show how to manage complexity by using layers of abstraction and base classes. By adapting these techniques, you will write more "reasonable" code, and build efficient and reusable verification components. Both a learning tool and a reference, this handbook contains hundreds of real-world code snippets and three professional verification-system examples. You can copy and paste from these examples, which are all based on an open-source, vendor-neutral framework (with code freely available at www.trusster.com). Learn about OOP techniques such as these: Creating classes—code interfaces, factory functions, reuse Connecting classes—pointers, inheritance, channels Using "correct by construction"—strong typing, base classes Packaging it up—singletons, static methods, packages

Describes a small verification library with a concentration on user adaptability such as re-useable components, portable Intellectual Property, and co-verification. Takes a realistic view of reusability and distills lessons learned down to a tool box of techniques and guidelines.

This advanced textbook presents an almost complete overview of techniques for hardware verification. It covers all approaches used in existing tools, such as binary and word-level decision diagrams, symbolic methods for equivalence and temporal logic model checking, and introduces the use of higher-order logic theorem proving for verifying circuit correctness. Each chapter contains an introduction and a summary as well as a section for the advanced reader, aiding an understanding of the advantages and limitations of each technique. Backed by many examples and illustrations, this text will appeal to a broad audience, from beginners in system design to experts. XXXXXXX Neuer Text This is a complete overview of existing techniques for hardware verification. It covers all approaches used in existing verification tools, such as symbolic methods for equivalence checking, temporal logic model checking, and higher-order logic theorem proving for verifying circuit correctness. The book helps readers to understand the advantages and limitations of each technique. Each chapter contains a summary as well as a section for the advanced reader.

These are the conference proceedings of the 4th Haifa Veri?cation Conference, held October 27–30, 2008 in Haifa, Israel. This international conference is a unique venue that brings together leading researchers and practitioners of both formal and dynamic veri?cation, for both hardware and software systems. This year's

conference extended the successes of the previous years, with a largejumpinthenumberofsubmitted papers. Wereceived49totalsubmissions, with many more high-quality papers than we had room to accept. Submissions came from 19 di?erent countries, re?ecting the growing international visibility of the conference. Of the 49 submissions, 43 were regular papers, 2 of which were later withdrawn, and 6 were tool papers. After a rigorous review process, in which each paper received at least four independent reviews from the dist- guished Program Committee, we accepted 12 regular papers and 4 tools papers for presentation at the conference and inclusion in this volume. These numbers give acceptance rates of 29% for regular papers and 67% for tool papers (34% combined) — comparable to the elite, much older, conferences in the ?eld. A Best Paper Award, selected on the basis of the reviews and scores from the Program Committee, was presented to Edmund Clarke, Alexandre Donz´ e, and AxelLegayfortheirpaperentitled"StatisticalModelCheckingofMixed-Analog Circuits with an Application to a Third-Order Delta-Sigma Modulator. " The refereed program was complemented by an outstanding program of - vited talks, panels, and special sessions from prominent leaders in the ?eld.

Hardware Verification with System Verilog

8th International Haifa Verification Conference, HVC 2012, Haifa, Israel, November 6-8, 2012. Revised Selected Papers

The e Hardware Verification Language

Embedded Software Verification and Debugging

10th International Conference, TACAS 2004, Held as Part of the Joint European Conferences on Theory and Practice of Software, ETAPS 2004, Barcelona, Spain, March 29 - April 2, 2004, Proceedings

First International Haifa Verification Conference, Haifa, Israel, November 13-16, 2005, Revised Selected Papers

This book constitutes the refereed proceedings of the Third International Conference on Formal Methods in Computer-Aided Design, FMCAD 2000, held in Austin, Texas in November 2000. The 30 revised full papers presented together with two invited contributions were carefully reviewed and selected from 63 submissions. All current issues of research and development approaches based on formal methods for the design and analysis of systems are addressed. Among the topics covered are formal verification, formal specification, systems analysis, program analysis, model checking, automated modeling, program semantics, theorem proving, symbolic simulation, and transition systems.

This book constitutes the thoroughly refereed proceedings of the 8th International Haifa Verification Conference, HVC 2012, held in Haifa, Israel in November 2012. The 18 revised full papers presented together with 3 poster presentations were carefully reviewed and selected from 36 submissions. They focus on the future directions of testing and verification for hardware, software, and complex hybrid systems.

I am glad to see this new book on the e language and on verification. I am especially glad to see a description of the e Reuse Methodology (eRM). The main goal of verification is, after all, finding more bugs quicker using given resources, and verification reuse (module-to-system, old-system-to-new-system etc.) is a key enabling component. This book offers a fresh approach in teaching the e hardware verification language within the context of coverage driven verification methodology. I hope it will help the reader und- stand the many important and interesting topics surrounding hardware verification. Yoav Hollander Founder and CTO, Verisity Inc. Preface This book provides a detailed coverage of the e hardware verification language (HVL), state of the art verification methodologies, and the use of e HVL as a facilitating verification tool in implementing a state of the art verification environment. It includes comprehensive descriptions of the new concepts introduced by the e language, e language syntax, and its as- ciated semantics. This book also describes the architectural views and requirements of verifi- tion environments (randomly generated environments, coverage driven verification environments, etc.), verification blocks in the architectural views (i. e. generators, initiators, c- lectors, checkers, monitors, coverage definitions, etc.) and their implementations using the e HVL. Moreover, the e Reuse Methodology (eRM), the motivation for defining such a gui- line, and step-by-step instructions for building an eRM compliant e Verification Component (eVC) are also discussed.

This volume contains the proceedings of the 3rd Haifa Veri?cation Conference (HVC 2007),whichtookplacein Haifa during October 2007.HVC isa forumfor researchers from both industry and academia to share and advance knowledge in the veri?cation of hardware and software systems. Academic research in veri?cation is generally divided into two paradigms – formal veri?cation and dynamic veri?cation (testing). Within each paradigm, di?erent algorithms and techniques are used for hardware and softwaresystems. Yet,attheircore,allofthesetechniquesaimtoachievethesamegoalofensuring the correct functionality of a complicated system. HVC is the only conference that brings together researchers from all four ?elds, thereby encouraging the migration of methods and ideas between domains. With this goal in mind we established the HVC Award. This award rec- nizes a promising contribution to veri?cation published in the last few years. It is aimed at developments that signi?cantly advance the state of the art in veri?cation technology and show potential for future impact on di?erent ver- cation paradigms. The winners of the HVC Award are chosen by an indep- dent committee with experts from all ?elds of veri?cation – both formal and dynamic, software and hardware. The winners of the 2007 HVC Award were Corina Pas? ? areanu and Willem Visser, for their work on combining static and dynamic analysis. This year we received 32 submissions, out of which 15 were accepted after a thorough review conducted by the Program Committee (PC) and additional reviewers.Eachpaper wasreviewedby atleastthree reviewers,sometimes more.

A Guide to Learning the Testbench Language Features

A Formal Hardware Verification System User's Guide

10th International Haifa Verification Conference, HVC 2014, Haifa, Israel, November 18-20, 2014, Proceedings

A SystemC Based Approach for Successful Tapeout

Hardware Verification with C++

Current Trends in Hardware Verification and Automated Theorem Proving

This book constitutes the thoroughly refereed post-conference proceedings of the 7th International Haifa Verification Conference, HVC 2011, held in Haifa, Israel in December 2011. The 15 revised full papers presented together with 3 tool papers and 4 posters were carefully reviewed and selected from 43 submissions. The papers are organized in topical sections on synthesis, formal verification, software quality, testing and coverage, experience and tools, and posters- student event.

This book constitutes the refereed post-proceedings of the First International Conference on Hardware Verification, Software Testing, and PADTAD held in November 2005. The conference combines the sixth IBM Verification Workshop, the fourth IBM Software Testing Workshop, and the third PADTAD (Parallel and Distributed Systems: Testing and Debugging) Workshop. The 14 revised full papers presented together with three invited contributions were carefully reviewed and selected from 31 submissions. The papers address all current issues in hardware/software verification, software testing, and testing of parallel and concurrent applications.

This report describes the partially completed correctness proof of the Viper 'block model'. Viper [7,8,9,11,23] is a microprocessor designed by W. J. Cullyer, C. Pygott and J. Kershaw at the Royal Signals and Radar Establishment in Malvern, England, (henceforth 'RSRE') for use in safety-critical applications such as civil aviation and nuclear power plant control. It is currently finding uses in areas such as the de ployment of weapons from tactical aircraft. To support safety-critical applications, Viper has a particulary simple design about which it is relatively easy to reason using current techniques and models. The designers, who deserve much credit for the promotion of formal methods, intended from the start that Viper be formally verified. Their idea was to model Viper in a sequence of decreasingly abstract levels, each of which concentrated on some aspect ofthe design, such as the flow ofcontrol, the processingofinstructions, and so on. That is, each model would be a specification of the next (less abstract) model, and an implementation of the previous model (if any). The verification effort would then be simplified by being structured according to the sequence of abstraction levels. These models (or levels) of description were characterized by the design team. The first two levels, and part of the third, were written by them in a logical language amenable to reasoning and proof.

This is the first book to focus on the problem of ensuring the correctness of floating-point hardware designs through mathematical methods. Formal Verification of Floating-Point Hardware Design advances a verification methodology based on a unified theory of register-transfer logic and floating-point arithmetic that has been developed and applied to the formal verification of commercial floating-point units over the course of more than two decades, during which the author was employed by several major microprocessor design companies. The book consists of five parts, the first two of which present a rigorous exposition of the general theory based on the first principles of arithmetic. Part I covers bit vectors and the bit manipulation primitives, integer and fixed-point encodings, and bit-wise logical operations. Part II addresses the properties of floating-point numbers, the formats in which they are encoded as bit vectors, and the various modes of floating-point rounding. In Part III, the theory is extended to the analysis of several algorithms and optimization techniques that are commonly used in commercial implementations of elementary arithmetic operations. As a basis for the formal verification of such implementations, Part IV contains high-level specifications of correctness of the basic arithmetic instructions of several major industry-standard floating-point architectures, including all details pertaining to the handling of exceptional conditions. Part V illustrates the methodology, applying the preceding theory to the comprehensive verification of a state-of-the-art commercial floating-point unit. All of these results have been formalized in the logic of the ACL2 theorem prover and mechanically checked to ensure their correctness. They are presented here, however, in simple conventional mathematical notation. The book presupposes no familiarity with ACL2, logic design, or any mathematics beyond basic high school algebra. It will be of interest to verification engineers as well as arithmetic circuit designers who appreciate the value of a rigorous approach to their art, and is suitable as a graduate text in computer arithmetic.

16th International Conference, CAV 2004, Boston, MA, USA, July 13-17, 2004, Proceedings

Advanced Verification Techniques

Correct Hardware Design and Verification Methods

Co-verification of Hardware and Software for ARM SoC Design

Tools and Algorithms for the Construction and Analysis of Systems

A Practitioner's Handbook

CHARME'99 is the tenth in a series of working conferences devoted to the dev- opment and use of leading-edge formal techniques and tools for the design and veri?cation of hardware and systems. Previous conferences have been held in Darmstadt (1984), Edinburgh (1985), Grenoble (1986), Glasgow (1988), Leuven (1989), Torino (1991), Arles (1993), Frankfurt (1995) and Montreal (1997). This workshop and conference series has been organized in cooperation with IFIP WG 10. 5. It is now the biannual counterpart of FMCAD, which takes place every even-numbered year in the USA. The 1999 event took place in Bad Her- nalb, a resort village located in the Black Forest close to the city of Karlsruhe. The validation of functional and timing behavior is a major bottleneck in current VLSI design systems. A predominantly academic area of study until a few years ago, formal design and veri?cation techniques are now migrating into industrial use. The aim of CHARME'99 is to bring together researchers and users from academia and industry working in this active area of research. Two invited talks illustrate major current trends: the presentation by G ?erard Berry (Ecole des Mines de Paris, Sophia-Antipolis, France) is concerned with the use of synchronous languages in circuit design, and the talk given by Peter Jansen (BMW, Munich, Germany) demonstrates an application of formal methods in an industrial environment. The program also includes 20 regular presentations and 12 short presentations/poster exhibitions that have been selected from the 48 submitted papers.

With our ever-increasing reliance on computer technology in every field of modern life, the need for continuously evolving and improving cyber security remains a constant imperative. This book presents the 3 keynote speeches and 10 papers delivered at the 2nd Singapore Cyber Security R&D Conference (SG-CRC 2017), held in Singapore, on 21-22 February 2017. SG-CRC 2017 focuses on the latest research into the techniques and methodologies of cyber security. The goal is to construct systems which are resistant to cyber-attack, enabling the construction of safe execution environments and improving the security of both hardware and software by means of mathematical tools and engineering approaches for the design, verification and monitoring of cyber-physical systems. Covering subjects which range from messaging in the public cloud and the use of scholarly digital libraries as a platform for malware distribution, to low-dimensional bigram analysis for mobile data fragment classification, this book will be of interest to all those whose business it is to improve cyber security.

This book presents the basis for reusing the test vector generation and simulation for the purpose of implementation verification, to result in a significant timesaving. It brings the results in the direction of merging manufacturing test vector generation and verification.

This book constitutes the thoroughly refereed post-proceedings of the Second International Haifa Verification Conference, HVC 2006, held in Haifa, Israel, in October 2006. The 15 revised full papers presented together with 2 invited lectures are organized in three topical tracks on hardware verification technologies and methodologies, software testing, and tools for hardware verification and software testing.

An Object-Oriented Framework

The Complete Industry Cycle

Formal Methods for Hardware Verification

Hardware/Software Co-Design and Co-Verification

Methodology and Techniques

Computer Aided Verification

This book is intended as an innovative overview of current formal verification methods, combined with an in-depth analysis of some advanced techniques to improve the scalability of these methods, and close the gap between design and verification in computer-aided design. Formal Verification: Scalable Hardware Verification with Symbolic Simulation explains current formal verification methods and provides an in-depth analysis of some advanced techniques to improve the scalability of these methods and close the gap between design and verification in computer-aided design. It provides the theoretical background required to present such methods and advanced techniques, i.e. Boolean function representations, models of sequential networks and, in particular, some novel algorithms to expose the disjoint support decompositions of Boolean functions, used in one of the scalable approaches.

This is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign-off. All the verification aspects in this exciting new book are illustrated with a single reference design for Bluetooth application.

This book constitutes the refereed proceedings of the 12th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods, CHARME 2003, held in L'Aquila, Italy in October 2003. The 24 revised full papers and 8 short papers presented were carefully reviewed and selected from 65 submissions. The papers are organized in topical sections on software verification, automata based methods, processor verification, specification methods, theorem proving, bounded model checking, and model checking and applications.

Hardware/software co-verification is how to make sure that embedded system software works correctly with the hardware, and that the hardware has been properly designed to run the software successfully -before large sums are spent on prototypes or manufacturing. This is the first book to apply this verification technique to the rapidly growing field of embedded systems-on-a-chip(SoC). As traditional embedded system design evolves into single-chip design, embedded engineers must be armed with the necessary information to make educated decisions about which tools and methodology to deploy. SoC verification requires a mix of expertise from the disciplines of microprocessor and computer architecture, logic design and simulation, and C and Assembly language embedded software. Until now, the relevant information on how it all fits together has not been available. Andrews, a recognized expert, provides in-depth information about how co-verification really works, how to be successful using it, and pitfalls to avoid. He illustrates these concepts using concrete examples with the ARM core - a technology that has the dominant market share in embedded system product design. The companion CD-ROM contains all source code used in the design examples, a searchable e-book version, and useful design tools. * The only book on verification for systems-on-a-chip (SoC) on the market * Will save engineers and their companies time and money by showing them how to speed up the testing process, while still avoiding costly mistakes * Design examples use the ARM core, the dominant technology in SoC, and all the source code is included on the accompanying CD-Rom, so engineers can easily use it in their own designs

Second International Haifa Verification Conference, HVC 2006, Haifa, Israel, October 23-26, 2006, Revised Selected Papers

A Mathematical Approach

Logic Synthesis and Verification

Hardware and Software, Verification and Testing

4th International Haifa Verification Conference, HVC 2008, Haifa, Israel, October 27-30, 2008, Revised Selected Papers

Proceedings of the 2nd Singapore Cyber-Security R&D Conference (SG-CRC 2017)

Based on the highly successful second edition, this extended edition of SystemVerilog for Verification: A Guide to Learning the Testbench Language Features teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill. In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students understanding of the material. Other features of this revision include: New sections on static variables, print specifiers, and DPI from the 2009 IEEE language standard Descriptions of UVM features such as factories, the test registry, and the configuration database Expanded code samples and explanations Numerous samples that have been tested on the major SystemVerilog simulators SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Third Edition is suitable for use in a one-semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level. Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers.

"As chip size and complexity continues to grow exponentially, the challenges of functional verification are becoming a critical issue in the electronics industry. It is now commonly heard that logical errors missed during functional verification are the most common cause of chip re-spins, and that the costs associated with functional verification are now outweighing the costs of chip design. To cope with these challenges engineers are increasingly relying on new design and verification methodologies and languages. Transaction-based design and verification, constrained random stimulus generation, functional coverage analysis, and assertion-based verification are all techniques that advanced design and verification teams routinely use today. Engineers are also increasingly turning to design and verification models based on C/C++ and SystemC in order to build more abstract, higher performance hardware and software models and to escape the limitations of RTL HDLs. This new book, Advanced Verification Techniques, provides specific guidance for these advanced verification techniques. The book includes realistic examples and shows how SystemC and SCV can be applied to a variety of advanced design and verification tasks." - Stuart Swan

Co-Design is the set of emerging techniques which allows for the simultaneous design of Hardware and Software. In many cases where the application is very demanding in terms of various performances (time, surface, power consumption), trade-offs between dedicated hardware and dedicated software are becoming increasingly difficult to decide upon in the early stages of a design. Verification techniques - such as simulation or proof techniques - that have proven necessary in the hardware design must be dramatically adapted to the simultaneous verification of Software and Hardware. Describing the latest tools available for both Co-Design and Co-Verification of systems, Hardware/Software Co-Design and Co-Verification offers a complete look at this evolving set of procedures for CAD environments. The book considers all trade-offs that have to be made when co-designing a system. Several models are presented for determining the optimum solution to any co-design problem, including partitioning, architecture synthesis and code generation. When deciding on trade-offs, one of the main factors to be considered is the flow of communication, especially to and from the outside world. This involves the modeling of communication protocols. An approach to the synthesis of interface circuits in the context of co-design is presented. Other chapters present a co-design oriented flexible component data-base and retrieval methods; a case study of an ethernet bridge, designed using LOTOS and co-design methodologies and finally a programmable user interface based on monitors. Hardware/Software Co-Design and Co-Verification will help designers and researchers to understand these latest techniques in system design and as such will be of interest to all involved in embedded system design.

This book constitutes the refereed proceedings of the 16th International Conference on Computer Aided Verification, CAV 2004, held in Boston, MA, USA, in July 2004. The 32 revised full research papers and 16 tool papers were carefully reviewed and selected from 144 submissions. The papers cover all current issues in computer aided verification and model checking, ranging from foundational and methodological issues to the evaluation of major tools and systems.

Using Testing Techniques in Hardware Verification

ESL Design and Verification

Formal Verification of Floating-Point Hardware Design

Vos

Third International Haifa Verification Conference, HVC 2007, Haifa, Israel, October 23-25, 2007, Proceedings

Introduction to Formal Hardware Verification

This state-of-the-art monograph presents a coherent survey of a variety of methods and systems for formal hardware verification. It emphasizes the presentation of approaches that have matured into tools and systems usable for the actual verification of nontrivial circuits. All in all, the book is a representative and well-structured survey on the success and future potential of formal methods in proving the correctness of circuits. The various chapters describe the respective approaches supplying theoretical foundations as well as taking into account the application viewpoint. By applying all methods and systems presented to the same set of IFIP WG10.5 hardware verification examples, a valuable and fair analysis of the strenghts and weaknesses of the various approaches is given.

Microprocessors increasingly control and monitor our most critical systems, including automobiles, airliners, medical systems, transportation grids, and defense systems. The relentless march of semiconductor process technology has given engineers exponentially increasing transistor budgets at constant recurring cost. This has encouraged increased functional integration onto a single die, as well as increased architectural sophistication of the functional units themselves. Additionally, design cycle times are decreasing, thus putting increased schedule pressure on engineers. Not surprisingly, this environment has led to a number of uncaught design flaws. Traditional simulation-based design verification has not kept up with the scale or pace of modern microprocessor system design. Formal verification methods offer the promise of improved bug-finding capability, as well as the ability to establish functional correctness of a detailed design relative to a high-level specification. However, widespread use of formal methods has had to await breakthroughs in automated reasoning, integration with engineering design languages and processes, scalability, and usability. This book presents several breakthrough design and verification techniques that allow these powerful formal methods to be employed in the real world of high-assurance microprocessor system design.

Hardware Verification with C++A Practitioner ' s HandbookSpringer Science & Business Media

Visit the authors' companion site! http://www.electronicsystemlevel.com/ - Includes interactive forum with the authors! Electronic System Level (ESL) design has mainstreamed – it is now an established approach at most of the world ' s leading system-on-chip (SoC) design companies and is being used increasingly in system design. From its genesis as an algorithm modeling methodology with ‘ no links to implementation ’ , ESL is evolving into a set of complementary methodologies that enable embedded system design, verification and debug through to the hardware and software implementation of custom SoC, system-on-FPGA, system-on-board, and entire multi-board systems. This book arises from experience the authors have gained from years of work as industry practitioners in the Electronic System Level design area; they have seen "SLD" or "ESL" go through many stages and false starts, and have observed that the shift in design methodologies to ESL is finally occurring. This is partly because of ESL technologies themselves are stabilizing on a useful set of languages being standardized (SystemC is the most notable), and use models are being identified that are beginning to get real adoption. ESL DESIGN & VERIFICATION offers a true prescriptive guide to ESL that reviews its past and outlines the best practices of today. Table of Contents CHAPTER 1: WHAT IS ESL? CHAPTER 2: TAXONOMY AND DEFINITIONS FOR THE ELECTRONIC SYSTEM LEVEL CHAPTER 3: EVOLUTION OF ESL DEVELOPMENT CHAPTER 4: WHAT ARE THE ENABLERS OF ESL? CHAPTER 5: ESL FLOW CHAPTER 6: SPECIFICATIONS AND MODELING CHAPTER 7: PRE-PARTITIONING ANALYSIS CHAPTER 8: PARTITIONING CHAPTER 9: POST-PARTITIONING ANALYSIS AND DEBUG CHAPTER 10: POST-PARTITIONING VERIFICATION CHAPTER 11: HARDWARE IMPLEMENTATION CHAPTER 12: SOFTWARE IMPLEMENTATION CHAPTER 13: USE OF ESL FOR IMPLEMENTATION VERIFICATION CHAPTER 14: RESEARCH, EMERGING AND FUTURE PROSPECTS APPENDIX: LIST OF ACRONYMS * Provides broad, comprehensive coverage not available in any other such book * Massive global appeal with an internationally recognised author team * Crammed full of state of the art content from notable industry experts

Formal Methods in Computer-Aided Design

13th IFIP WG 10.5Advanced Research, Working Conference, CHARME 2005, Saarbrücken, Germany, October 3-6, 2005, Proceedings

Hardware Design Verification

10th IFIP WG10.5 Advanced Research Working Conference, CHARME'99, Bad Herrenalb, Germany, September 27-29, 1999, Proceedings

Hardware and Software: Verification and Testing

A Prescription for Electronic System Level Methodology

The Practical, Start-to-Finish Guide to Modern Digital Design Verification As digital logic designs grow larger and more complex, functional verification has become the number one bottleneck in the design process. Reducing verification time is crucial to project success, yet many practicing engineers have had little formal training in verification, and little exposure to the newest solutions.Hardware Design Verificationsystematically presents today's most valuable simulation-based and formal verification techniques, helping test and design engineers choose the best approach for each project, quickly gain confidence in their designs, and move into fabrication far more rapidly. College students will find that coverage of verification principles and common industry practices will help them prepare for jobs as future verification engineers. Author William K. Lam, one of the world's leading experts in design verification, is a recent winner of the Chairman's Award for Innovation, Sun Microsystems' most prestigious technical achievement award. Drawing on his wide-ranging experience, he introduces the foundational principles of verification, presents traditional techniques that have survived the test of time, and introduces emerging techniques for today's most challenging designs. Throughout, Lam emphasizes practical examples rather than mathematical proofs; wherever advanced math is essential, he explains it clearly and accessibly. Coverage includes Simulation-based versus formal verification: advantages, disadvantages, and tradeoffs Coding for verification: functional and timing correctness, syntactical and structure checks, simulation performance, and more Simulator architectures and operations, including event-driven, cycle-based, hybrid, and hardware-based simulators Testbench organization, design, and tools: creating a fast, efficient test environment Test scenarios and assertion: planning, test cases, test generators, commercial and Verilog assertions, and more Ensuring complete coverage, including code, parameters, functions, items, and cross-coverage The verification cycle: failure capture, scope reduction, bug tracking, simulation data dumping, isolation of underlying causes, revision control, regression, release mechanisms, and tape-out criteria An accessible introduction to the mathematics and algorithms of formal verification, from Boolean functions to state-machine equivalence and graph algorithms Decision diagrams, equivalence checking, and symbolic simulation Model checking and symbolic computation Simply put,Hardware Design Verificationwill help you improve and accelerate your entire verification process--from planning through tape-out--so you can get to market faster with higher quality designs.

One of the biggest challenges in chip and system design is determining whether the hardware works correctly. That is the job of functional verification engineers and they are the audience for this comprehensive text from three top industry professionals. As designs increase in complexity, so has the value of verification engineers within the hardware design team. In fact, the need for skilled verification engineers has grown dramatically--functional verification now consumes between 40 and 70% of a project's labor, and about half its cost. Currently there are very few books on verification for engineers, and none that cover the subject as comprehensively as this text. A key strength of this book is that it describes the entire verification cycle and details each stage. The organization of the book follows the cycle, demonstrating how functional verification engages all aspects of the overall design effort and how individual cycle stages relate to the larger design process. Throughout the text, the authors leverage their 35 plus years experience in functional verification, providing examples and case studies, and focusing on the skills, methods, and tools needed to complete each verification task. Comprehensive overview of the complete verification cycle Combines industry experience with a strong emphasis on functional verification fundamentals Includes real-world case studies

This book constitutes the refereed proceedings of the 10th International Haifa Verification Conference, HVC 2014, held in Haifa, Israel, in November 2014. The 17 revised full papers and 4 short papers presented were carefully reviewed and selected from 43 submissions. The papers cover a wide range of topics in the sub-fields of testing and verification applicable to software, hardware, and complex hybrid systems.

Research and development of logic synthesis and verification have matured considerably over the past two decades. Many commercial products are available, and they have been critical in harnessing advances in fabrication technology to produce today's plethora of electronic components. While this maturity is assuring, the advances in fabrication continue to seemingly present unwieldy challenges. Logic Synthesis and Verification provides a state-of-the-art view of logic synthesis and verification. It consists of fifteen chapters, each focusing on a distinct aspect. Each chapter presents key developments, outlines future challenges, and lists essential references. Two unique features of this book are technical strength and comprehensiveness. The book chapters are written by twenty-eight recognized leaders in the field and reviewed by equally qualified experts. The topics collectively span the field. Logic Synthesis and Verification fills a current gap in the existing CAD literature. Each chapter contains essential information to study a topic at a great depth, and to understand further developments in the field. The book is intended for seniors, graduate students, researchers, and developers of related Computer-Aided Design (CAD) tools. From the foreword: "The commercial success of logic synthesis and verification is due in large part to the ideas of many of the authors of this book. Their innovative work contributed to design automation tools that permanently changed the course of electronic design." by Aart J. de Geus, Chairman and CEO, Synopsys, Inc.

6th International School on Formal Methods for the Design of Computer, Communication, and Software Systems, SFM 2006, Bertinoro, Italy, May 22-27, 2006, Advances Lectures

System-on-a-Chip Verification

12th IFIP WG 10.5 Advanced Research Working Conference, CHARME 2003, L'Aquila, Italy, October 21-24, 2003, Proceedings

SystemVerilog for Verification

Third International Conference, FMCAD 2000 Austin, TX, USA, November 1-3, 2000 Proceedings

This book constitutes the refereed proceedings of the 13th International Haifa Verification Conference, HVC 2017, held in Haifa, Israel in November 2017.The 13 revised full papers presented together with 4 poster and 5 tool demo papers were carefully reviewed and selected from 45 submissions. They are dedicated to advance the state of the art and state of the practice in verification and testing and are discussing future directions of testing and verification for hardware, software, and complex hybrid systems.

This book constitutes the refereed proceedings of the 13th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods, CHARME 2005, held in Saarbrücken, Germany, in October 2005. The 21 revised full papers and 18 short papers presented together with 2 invited talks and one tutorial were carefully reviewed and selected from 79 submissions. The papers are organized in topical sections on functional approaches to design description, game solving approaches, abstraction, algorithms and techniques for speeding (DD-based) verification, real time and LTL model checking, evaluation of SAT-based tools, model reduction, and verification of memory hierarchy mechanisms.

Simulation and Formal Method-based Approaches

11th IFIP WG 10.5 Advanced Research Working Conference, CHARME 2001 Livingston, Scotland, UK, September 4-7, 2001 Proceedings

Methods and Systems in Comparison

7th International Haifa Verification Conference, HVC 2011, Haifa, Israel, December 6-8, 2011, Revised Selected Papers

Design and Verification of Microprocessor Systems for High-Assurance Applications